ABSTRACT OF THE DISCLOSURE

A clock synthesis circuit (22) including a phase-locked loop (25) and one or more frequency synthesis circuits (27; 77; 227; 237) is disclosed. A disclosed implementation of the phase-locked loop (25) includes a voltage-controlled oscillator (30) having an even number of differential stages (31) to produce an even number of equally spaced clock phases. In one arrangement, the frequency synthesis circuit (27) includes two adder legs that generate select signals applied to first and second multiplexers (40a, 40b), for selecting among the clock phases from the voltage-controlled oscillator (30). The outputs of the first and second multiplexers (40a, 40b) are applied to a two-to-one multiplexer (46) which is controlled by the output clock signal (CLK1), to drive clock edges to a T flip-flop (48) to produce the output clock signals (CLK1, CLK2). In another embodiment, more than two adder and register units (55) control corresponding multiplexers (56) for selecting clock phases from the voltage-controlled oscillator (30) for application to an output multiplexer (58), which is controlled by a clock control circuit (60) to apply the selected clock phases to the T flip-flop (62). In another embodiment, primary and phase-shifted frequency synthesis circuits (227, 327) receive initialization values (INIT1, INIT2) that establish the phase differential and ensure proper initialization.